Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

6. A flash memory, comprising:

a plurality of floating gate transistors, each transistor having a control gate a floating gate, a drain and a source, said plurality arranged in an N-row by M-column array, where N and M are integers greater than or equal to one;

N word lines, each word line connecting together the control gates of transistors in a common and corresponding row; and

M bit lines, each bit line connecting together the drains of transistors in a common and corresponding column,

wherein a specific floating gate transistor of the plurality is selected and programmed by applying a first voltage to the control gates of the transistors in the row in which the specific transistor is disposed, applying a second voltage to the source of the specific transistor and grounding the drain of the specific transistor.

7. The flash memory of claim 6, wherein the sources of all transistors are connected together as a common source.

8. The flash memory of claim 6, wherein the second voltage is greater than ground potential.

9. The flash memory of claim 6, wherein the source of each transistor comprises a first doped region having a first conductivity type extending into a semiconductor substrate having a second conductivity type of a charge opposite to the first conductivity type, thereby forming a first p-n junction.

10. The flash memory of claim 9, wherein the drain of each transistor comprises a second doped region of the first conductivity type, which is laterally spaced from the first doped region and extends into the substrate, thereby forming a second p-n junction.

11. The flash memory of claim 10, wherein the first doped region is a double-diffused region comprising a first sub-region of a first dopant species and a second sub-region of a second dopant species, the first and second dopant species being of the first conductivity type.

12. The flash memory of claim 11, wherein the first doped region extends deeper into the substrate than the second doped region.

13. The flash memory of claim 12, wherein the floating gate of each transistor is disposed vertically above and interposed between an oxide layer and the substrate such that the first doped region horizontally overlaps the floating gate to a greater extent than a horizontal overlap of the second doped region.

14. A non-volatile device, comprising:

a substrate;

a floating gate overlying the substrate;

a control gate overlying the floating gate and being electrically coupled to a word line extending in a first direction;

a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first graded profile and being electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and

a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second graded profile that is more sloped than the first graded profile,

wherein the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device.

15. The device of claim 14, wherein the drain region is grounded to program the non-volatile device.

16. The device of claim 15, wherein the source region is a double-diffused region including first and second species.

17. The device of claim 16, wherein the first species is arsenic and the second species is phosphorous.

18. The device of claim 15, wherein the first voltage is about 8.5 volts and the second voltage is about 4.5 volts.

19. A non-volatile semiconductor device, comprising:

a semiconductor substrate; and

a transistor formed on the substrate, the transistor including:

a floating gate overlying a surface of the substrate,

a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction,

a first conductive region provided in the substrate and proximate a first end of the floating gate, the first conductive region extending a first distance into the substrate and having a first graded profile relative to the surface of the substrate, the first conductive region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and

a second conductive region provided in the substrate and proximate a second end of the floating gate, the second conductive region being a double-diffused region that extends a second distance into the substrate and having a second graded profile relative to the surface of the substrate, the second distance being greater than the first distance, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile,

wherein the control gate is applied with a first voltage and the second conductive region is applied with a second voltage to program the non-volatile device, the second voltage being a positive voltage.

20. The device of claim 19, wherein the first conductive region is grounded to program the non-volatile device.

21. The device of claim 19, wherein the transistor is one of a plurality of cells formed on the substrate, the plurality of cells being arranged in an array of N rows and M

columns, each of the plurality of cells being configured to be programmed to a first conductive state or a second conductive state.

22. The device of claim 19, wherein the second conductive region includes first and second species.

23. The device of claim 22, wherein the first species is arsenic and the second species is phosphorous.

24. The device of claim 19, wherein the first distance is about 0.1 micron and the second distance is about 0.3 micron.

25. The device of claim 19, wherein the second distance is about three times greater than the first distance.